# CPRE 4910 Weekly Report 08

***11/11/2025 - 11/18/2025***

***Group number: SDMay26-24***

***Project title: Digital ASIC Fabrication***

***Client &/Advisor: Dr.  Henry Duwe***

***Team Members/Role:***

| | |
|---|---|
| ***Colin McGann*** | ***-Project Lead*** |
| ***Samuel Forde*** | ***-PCB & Layout Lead*** |
| ***Michael Drobot*** | ***-Firmware Lead*** |
| ***Jack Tonn*** | ***-Testbench and Validation Lead*** |
| ***Dawud Benedict*** | ***-Toolflow Lead*** |
| ***Emil Kosic*** | ***-Repository and Coding Standards Lead*** |
| ***Joshua Arceo*** | ***-Client/Advisor Communications Lead*** |

- **Weekly Summary**

  This week we presented our improved diagram showing how data will flow. There was a heavy emphasis on memory, caching, and core implementation.

- **Past Week Accomplishments**
  - Colin McGann: Finished up the SPI memory rewrite and started testing work for the pipelined divider.
  - Jack Tonn: Started implementing updated ISA and flow into the cores, researched previous predicated execution methods present in the cpre 581 course. I found that they are not useful in our case, but we can take inspiration from them to make minor changes.
  - Dawud Benedict: Rethinking cache design without coherency issues. Changed prefetch to SW activated. Thinking through HDL implementation.
  - Michael Drobot: Wrote core simulator, implemented extra instructions from ISA, refactored scripts folder to share more common code, and wrote design doc testing section.

- Sam Forde: Wrote verification for pipelined divider. Working on integrating commercial SRAM into design.
- Josh Arceo: Analyzed the reuse patterns, worked on verilog code for cache design
- Emil Kosic: Began performance metric research on cores

- **Pending Issues**
  - Research if the ISA is complete for the users, but not to feature creepy
    - Requires CC instructions including prefetch.
  - Reexamine caching structure, potentially cache pre-shaded vertices.
- **Individual contributions**

| NAME | Individual Contributions | Hours this week | HOURS cumulative |
|---|---|---|---|
| Colin McGann | FPGA and SPI memory controller work | 10 | 120 |
| Jack Tonn | ALU HDL and predication | 5 | 56 |
| Dawud Benedict | Cache design and memory hierarchy | 8 | 56 |
| Michael Drobot | Core simulator, design doc testing section | 25 | 120 |
| Sam Forde | Pipelined divider, commercial SRAM | 5 | 51 |
| Josh Arceo | Analyzed reuse scripts, figured out cache block size | 3 | 35 |
| Emil Kosic | Core global and local registers | 3 | 37 |

- **Plans for the upcoming week**
  - Colin McGann: Will continue working on our FPGA design and integrating the pipelined divider. Once this is done, I will have time to work on fixing timing in the FPGA.
  - Jack Tonn: Update design document & start working on faculty presentation
  - Dawud Benedict: Help with CC ISA. Working on the Verilog for the cache systems.
  - Michael Drobot: Keep the ISA updated, test all existing shader programs. Write fixed point division procedure for cores. Keep working on the core controller.
  - Sam Forde: Put together some performance analyses once mac test units have synthesized and area values are apparent.
  - Josh Arceo: Finish Verilog for cache, maybe create a simulation of the cache to run on our obj files
  - Emil Kosic: Continue performance analysis of cores, provide metrics to document

- **Advisor Meeting Summary**

Advisor/Client is worried about cache complexity. Based on his feedback, the cache should be as simple as possible moving forward, only using 1 level. Additionally, dynamic prefetching can get difficult and can be simplified as an instruction. For this project, pushing some work onto software instead of figuring it out in hardware can help prevent issues due to complexity.